ESD Simulation with Wunsch-Bell based Behavior Modeling Methodology

Yiqun Cao (1, 2), Ulrich Glaser (1), Joost Willemen (1), Filippo Magrini (1),

Michael Mayerhofer (1), Stephan Frei (2), Matthias Stecher (1)

(1) Infineon Technologies, Am Campeon1-12, D-85579, Neubiberg, Germany
tel.: +49 89 234 63936, E-mail: yiqun.cao@infineon.com

(2) Technische Universität Dortmund, Campus Nord, ET-Geb., Friedrich-Wöhler-Weg 4, D-44227, Dortmund, Germany

Abstract − Conventional modeling methods for ESD protection can be specific to device types or cannot reproduce the self-heating effect. This work proposes a straightforward modeling methodology based on the Wunsch-Bell characterization method using TLP. It allows precise ESD simulation verified by measurements.

I. Introduction

Traditional simplified models of on-chip ESD devices and structures reproduce their quasi-static I/V characteristics without concerning self-heating during ESD [1, 2]. In fact, as given by the Wunsch-Bell theory, the failure levels (failure power and failure energy) of semiconductor structures due to thermal run-away strongly depend on the pulse width (t_w) [3]. The power to failure as function of pulse width has different slopes between adiabatic region and Wunsch-Bell region according to the Dwyer's work [4]. In the ESD concepts, the ESD protection elements are designed to be firstly damaged above the ESD target level, and the modeling of ESD protection elements up to the high-current density regime or up to the failure level is of prime importance. Besides the failure levels, also the on-resistance (R_{on}) which directly affects the transient response of the ESD protections differs significantly because of self-heating when the ESD elements are carrying different pulse energies with different pulse durations. In fact, the ESD requirements of the semiconductor products have become very manifold nowadays. Due to different ESD standards from CDM, HBM to system-level ESD with various pulse forms one has to expect different behavior of the ESD structures with respect to self-heating. Further, the robustness of ESD elements stressed by pulses which are even beyond ESD range such as EOS pulses has also gained increasing interest [5, 6]. Hence the thermal effects and the modification of R_{on} in terms of stress duration need to be taken into account for the modeling issues.

Apart from many compact physical models which are available for SPICE simulation [7-11], this work introduces a novel Wunsch-Bell based behavior modeling methodology which basically considers the ESD structure or protected I/O pin as a black-box. As the electro-thermal simulation or thermal equivalent circuits often required for physics-based models are not necessary any more in the proposed behavior modeling method, technology parameters and device geometries are out of concern simplifying the modeling significantly. I/V properties as well as the failure levels of the device of interest can be simply characterized with TLP in a wide pulse range. The behavior modeling itself is language-independent. VHDL-AMS is chosen in this work for modeling. In prior publications, the behavior modeling methodologies using ETABLE operator [12] or
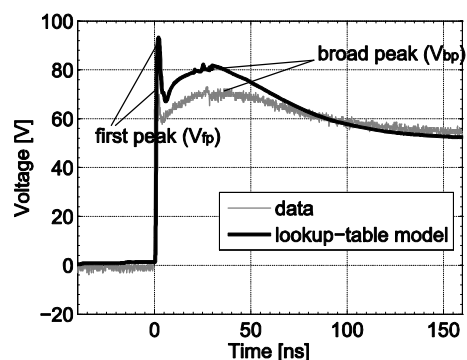

Figure 1: Simulated and measured voltage response of the pn-diode stressed with GUN-like pulse at 2kV level. Corresponding current waveforms (not shown here) match very well due to the well modeled current source.

lookup-table [13] focus mainly on the device characterizations with 100ns TLP. They can have very good usage for ESD simulation if self-heating in the protection elements is negligible. It is however shown in [14] with 100ns TLP characteristic only, that the model quality is not satisfying if an IEC 61000-4-2 [15] system-level ESD pulse (hereafter called GUN pulse) is applied to the modeled pn-diode (Fig. 1). For the stress-level higher than 2kV, the deviation of measurement data and model becomes even larger.

The modeling method in this work focuses on the one hand on the self-heating behavior and enables on the other hand the prediction of the robustness of the protection structures under various ESD stresses. The detailed modeling methodology is described in section II. Since the individual physical details are not required, the proposed methodology can be generally applied to model different types of ESD devices or protection networks. Three modeling examples for various types of ESD protections are introduced in section III. In addition, ESD simulation is performed in the co-design of on- and off-chip ESD protections to estimate their robustness in section IV. System-level ESD tests confirm the simulation results.

II. Modeling Methodology

Aiming at successful ESD simulations, the model has to reproduce the transient responses of the ESD elements at first. Based on that, the power and energy dissipated in the modeled devices can be accurately calculated from correctly simulated voltage and current waveforms. The failure or the robustness of
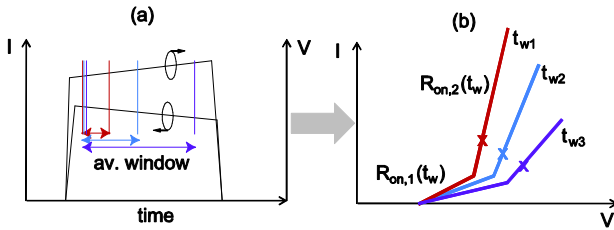

Figure 2: Based on (a) TLP characterization using the average windows of t_{w1}, t_{w2} and t_{w3}, (b) $R_{on, 1}$ and $R_{on, 2}$ are derived from averaged voltage and current transients as functions of t_w.
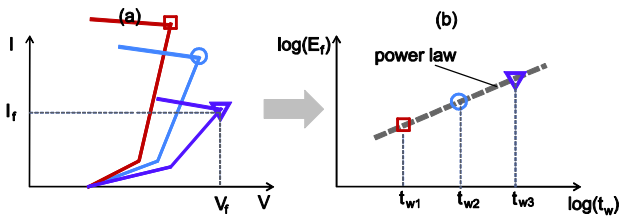

Figure 3: E_f as function of t_w (b) derived from failure current and voltage in TLP characteristics (a).

the ESD structure is then well predictable.

In this work, the ESD devices are characterized using Infineon TLP equipment with t_w from 5ns to 1.5µs. It aims to cover a wide pulse range from component- to system-level ESD requirements. Fig.2 illustrates schematically the TLP characterization for a breakdown device using different pulse widths. The characterization method as well as the measurement setup is similar as described in [10]. In Fig. 2, the modeling principle is qualitatively shown based on a breakdown ESD device with two linear on-resistances $R_{on, 1}$ and $R_{on, 2}$. In practical cases, more than two R_{on} can be defined depending on the complexity of the device behavior and the target model accuracy. I/V curves derived from the different average windows correspond to different pulse durations t_{w1}, t_{w2} and t_{w3}. The calculated I/V point from the current and voltage transients in Fig. 2 (a) is marked in Fig. 2 (b) for each t_w. Note that with self-heating, the voltage across the device increases with increasing pulse width while the current decreases. Self-heating takes noticeable effect showing t_w-dependent R_{on}. The device modeling reflects this device behavior by using a fitting function $R_{on}=f(t_w)$ within a linear segment of the I/V curves. In this example, two R_{on} ($R_{on, 1}$ and $R_{on, 2}$) as functions of t_w are modeled. The quality of the R_{on} fitting functions relies on the numbers of t_w used in the TLP characterization.

During the simulation, R_{on} is modified for every time step taking the effective pulse width into account:

$$R_{on,t_1} = R_{on}(t_w = t_1 - t_0)$$

where t_1 is the present time instant and t_0 is the ESD device turn-on time which is detected by the model. A time instant is considered as t_0 when the current through the modeled ESD element exceeds a pre-defined limit or the voltage across the modeled ESD element reaches the trigger voltage (V_{tr}). Hence t_0 is in general not equal to the start time of the pulse generation. The present voltage and current values $V(t_1)$ and $I(t_1)$ are self-consistently calculated by the simulator with the appropriate $R_{on,t1}$.

Fig. 3 illustrates the principle of building the thresholds of power to failure (P_f) or energy to failure (E_f) into the model with the fitting functions $P_f=f(t_w)$ or $E_f=f(t_w)$. A power law is adequate for devices such as pn-diodes within the Wunsch-Bell region [16]. In the simulation, the failure level limit at t_1, $E_{f, t1}$, is given by the energy $E_f(t_w=t_1-t_0)$. The energy dissipated in the device is calculated as

$$E_{t_1} = \int_{t=t_0}^{t=t_1} I(t) \cdot V(t) dt$$

```
begin
Ron1=F1(t); Ron2=F2(t);...
E=integ(V*I); Ef=F3(t);

if E<Ef use
        if I1>I>I0 use
        R=Ron1;
        V=F4(I,Ron1);
        elsif I2>I>I1 use
        R=Ron2;
        V=F5(I,Ron2);
        elsif ...
        ...
else
        Device is damaged!
end
```

Figure 4: Simplified VHDL-AMS modeling flow in Wunsch-Bell based behavior model. The switch conditions for fitting functions are the currents. Also voltage levels could be used as switch conditions.

The modeled device is considered as thermally damaged if the condition $E_{tl}<E_f(t_w)$ is violated at time. Fig. 4 gives the simplified modeling flow where all the fitting functions are defined by the Wunsch-Bell characterization. Note that by means of Wunsch-Bell characterization, the choice of the pulse duration is not only limited to the Wunsch-Bell region. The fitting function of failure power does not have to follow the power law. In addition, for ESD structures eventually having electrical limits such as active clamps [16], maximal allowed power (P_{max}) is used as the additional failure criterion.

III. Models of ESD Structures

A.pn-Diode

Pn-diodes belong to very simple but also very effective and reliable non-snapping ESD protection devices. Fig.5 shows the TLP characteristics of a 45V pn-diode. Key parameters included in the behavior model are the trigger voltage, on-resistances R1, R2 and R3 for the three different linear segments within one I/V curve. The thresholds for R_{on} switching determine the transition between R1, R2 and R3. In this specific example, the switching from R1 to R2 happens at the same current level regardless of the pulse width which implies that the current density is responsible for this transition. The current around 10A is used as the threshold between R2 and R3. The failure criterion is described with E_f since the investigated stand-alone pn-diode fails thermally. Fig. 6 shows the fitting functions of the parameters depending on t_w. For the pn-diode, 8 different pulse durations are chosen in the characterization which
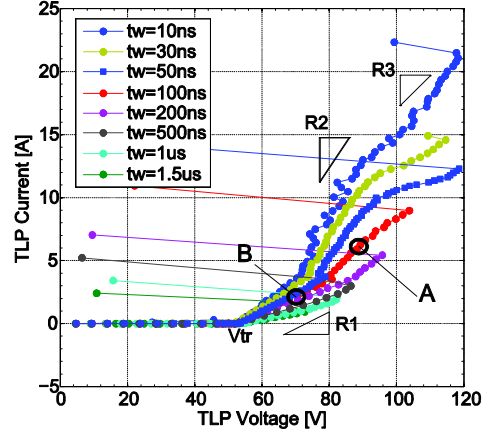
Figure 5: TLP characteristic of a 45V pn-diode with t_w from 10ns to 1.5μs. R1 to R3 represent different R_{on} in three segments of I/V curves as approximation. Each of R_{on} is a function of t_w.

delivers eight data points for building the function $E_f(t_w)$ and $R1(t_w)$. For R2 and R3, there are less data points because the pn-diode does not reach the thresholds of corresponding R_{on} transitions in case of longer pulses.

TLP simulation is the first step to verify the proposed modeling methodology. A good agreement of model and data is expected because the modeling itself is based on the TLP characterization. The results of the simulated and measured transient waveforms show
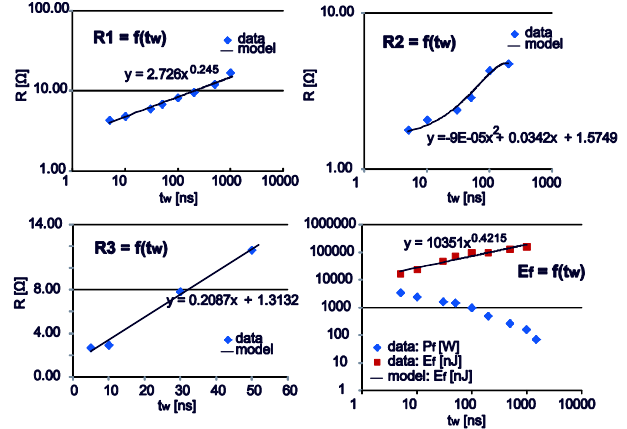
Figure 6: Fitting functions of the key parameters for the modeling of the pn-diode using TLP characterization.
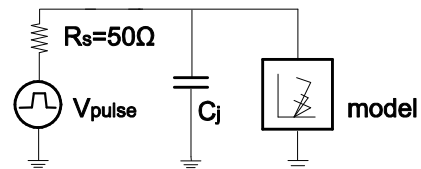
Figure 7: Simplified TLP simulation setup to perform the comparison of data and model. C_j is the junction capacitance of the DUT which amounts 2pF for the pn-diode.
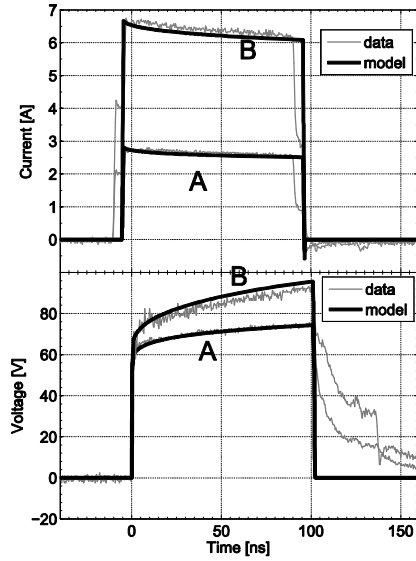
Figure 8: Comparison of Wunsch-Bell based model and TLP data with respect to transient responses of the pn-diode for t_w=100ns. "A" and "B" denote the corresponded I/V waveforms.
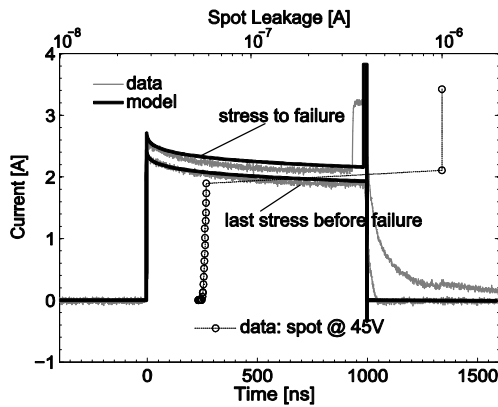

Figure 9: Comparison of Wunsch-Bell based model and TLP data for 1 μs TLP regarding the failure levels of the pn-diode.

excellent agreement with a wide range of pulse durations. Fig. 7 depicts the schematic of a very simplified TLP setup in the simulation. Fig.8 shows exemplary the simulated transients overlapped by the experimental results for 100ns TLP. The corresponding I/V pairs ("A" and "B") are marked in Fig. 5. Note the different levels of self-heating in the pn-diode in low and high current density regions. In addition to the waveform comparison, Fig. 9 shows that the behavior model reproduces also the failure levels. A 1 μs TLP pulse is taken as an example. The waveforms of the last stress before failure and the failing stress clearly show the correct estimation of the simulated failure levels. As soon as the device is considered as damaged, the model will switch the ESD device to low impedance (e.g. 1Ω) to represent nearly a short after device failure. As a result, the
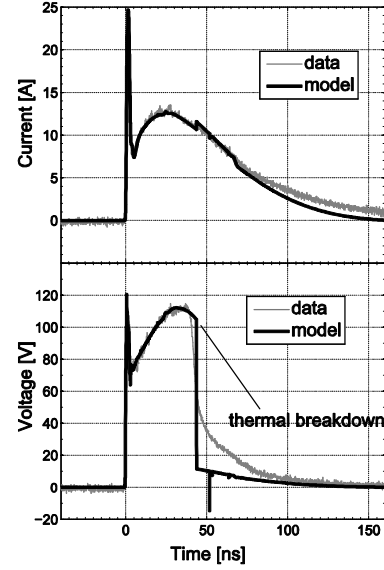

Figure 10: Simulated and measured waveforms for the pn-diode stressed by GUN-like pulses at 6kV stress level (stress to failure). Thermal destruction is observed both in simulation and measurement.

current and voltage transients will change abruptly in the simulation and the device failure can be easily distinguished in the simulated waveforms. Error or warning message is certainly delivered as well.

In addition to the TLP simulation, ESD-like pulses with non-square waveform are more practical and convincing for the validation of the modeling method. Fig. 10 compares the failure levels of the pn-diode stressed by GUN-like pulses applying wafer-level tests [17]. The same failure current is found in simulation and measurement. Moreover, the voltage transients clearly show the improved reproduction capability of the proposed modeling methodology including self-heating compared to the 100ns TLP based method in Fig. 1.

B. Active Clamp

Standard active clamps as a type of non-snapping high-voltage ESD protection circuits have gained increasing attention recently [16, 18]. As discussed, the Wunsch-Bell based methodology can easily be adapted to various types of protection elements without the deep knowledge of physical details. Nevertheless, the understanding of the device behavior is also essential. The main difference of the Zener-triggered active clamps compared to the pn-diodes from a modeling aspect is the transient turn-on behavior with respect to the capacitive gate coupling. The Zener-trigger defines the static trigger voltage of the active clamp. The DMOS transistor is designed to turn on and conduct ESD current for $V_{DS}>V_{tr}$. The
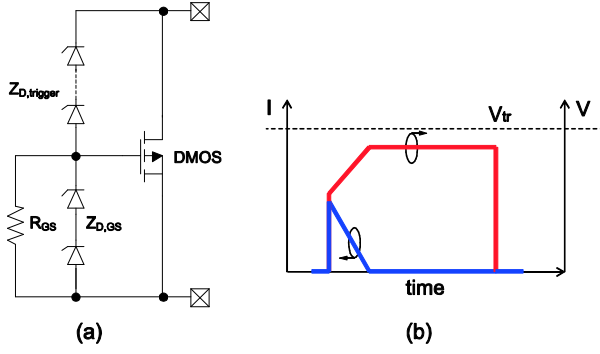
Figure 13: Comparison of Wunsch-Bell based model and TLP data with respect to transient responses of the active clamp. "A", "B" and "C" denote the corresponded I/V waveforms.

Figure 11: (a) The schematic of a Zener-triggered active clamp with gate discharge resistor R_{GS} and gate protection $Z_{D,GS}$. (b) The transient turn-on of the DMOS due to gate coupling showing typical I/V waveforms when the stress voltage is below the designed V_{tr}.

transistor is supposed to be off if V_{DS} does not exceed V_{tr}. However for $V_{DS}<V_{tr}$ the capacitive coupled gate-source voltage can still turn on the transistor transiently. After the $R_{GS}C_{GS}$ discharging, the transistor is turned off when V_{GS} goes below the threshold voltage of the DMOS. Fig. 11 shows the schematic of the active clamp circuitry as well as the transient turn-on behavior illustrated with the TLP waveforms for $V_{DS}<V_{tr}$.

Spectre modeling approach [16] could be involved to accurately model the parasitic capacitances and the DMOS transistor. The consideration of self-heating under ESD conditions would be very complicated this way. In the contrary, the proposed behavior modeling in this work assumes that the active clamp exhibits a finite on-resistance for $V<V_{tr}$ under short pulses. This effectively translates the transient turn-on of the active clamps into a t_w dependent R_{on}. Fig. 12 shows the TLP characteristics of a 25V active clamp: here R1 is

defined for the segment between 0V and V_{tr}. Fig. 13 shows the agreement of data and model for 100ns TLP with different voltage and current pairs indicated in Fig. 12.

For the failure estimation of the active clamps, P_{max} is built in the model as electrical limit in addition to E_f. Simulation and measurement with GUN-like pulses confirms the prediction of the electrically induced
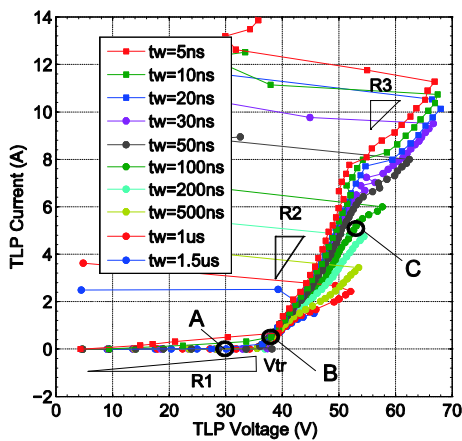

Figure 12: TLP characteristic of a 25V active clamp with t_w from 5ns to 1.5μs. R1 represents the transient turn-on behavior of active clamp where R2 and R3 represent different R_{on} after V_{tr} is reached.
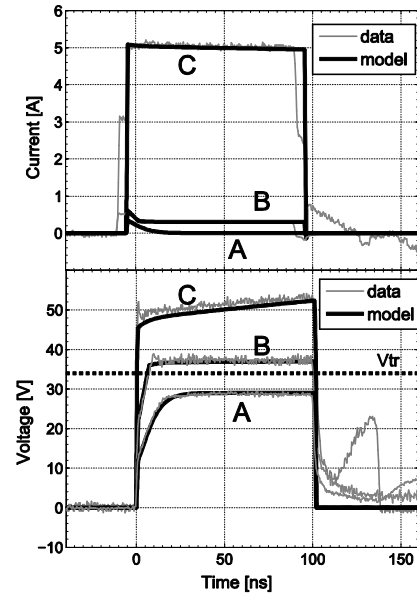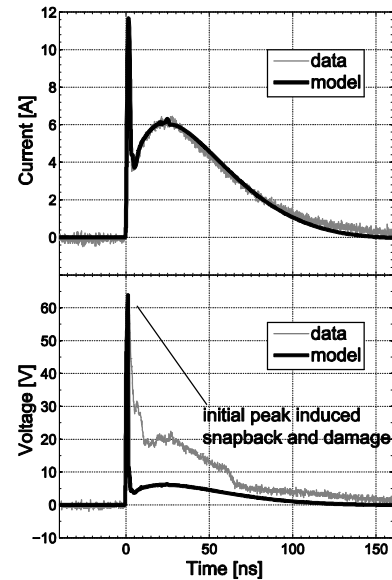

Figure 14: Simulated and measured waveforms for the active clamp stressed by GUN-like pulses at 3kV GUN level (stress to failure). Electrical failure is observed both in simulation and measurement.

failure and the failure level as shown in Fig. 14. Note that the transient voltage after the device damage is not meant to be correctly modeled. The silicon melting in the device after damage exhibits a time dependent degradation leading to leakage increase. In the simulation however, the device model is simply switched to a 1Ω resistance to identify the failure.

C. npn-BJT

Modeling of snapping ESD structures often encounters convergence problems in simulations. However, the behavior modeling methodology can be applied to snapping ESD elements without suffering from convergence issues. An npn-BJT implemented in a power technology is used as the third modeling example exhibiting a snapback characteristic. The TLP characteristics with diverse pulse durations are shown in Fig. 15. Note that for t_w=5ns, the holding voltage V_h seems to be larger than for larger t_w. This is caused by the snapback process of the bipolar transistor which takes several nanoseconds. The transient snapback from the trigger voltage to the holding voltage can last longer than 5ns. The averaged voltage is thus larger than the real V_h in the steady clamping state. Similar to the modeling of the transient turn-on behavior of active clamps, the virtual t_w-dependence of V_h can be utilized in the modeling to reproduce the snapback process of the device. With this consideration, one can use the proposed methodology to implement behavior models for snapping ESD devices with complex turn-on and self-heating effects. Fig. 16 confirms the agreement between model and measurement data with respect to transient waveforms in 100ns TLP. "A" to "C" indicate again the voltage and current waveforms corresponding to the I/V points in the TLP
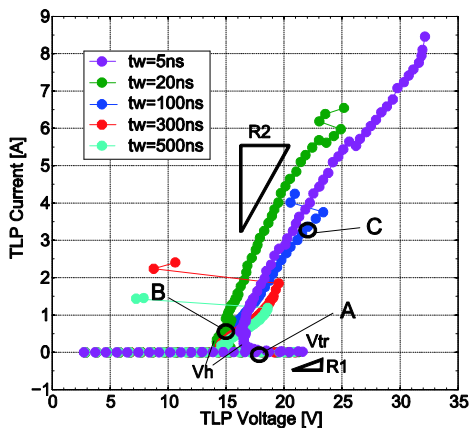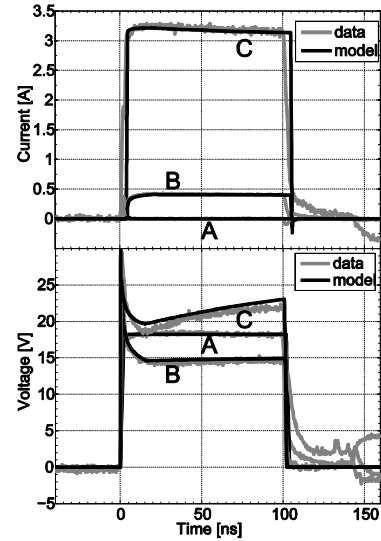

Figure 16: Comparison of Wunsch-Bell based model and TLP data regarding transient responses of the npn-BJT. "A", "B" and "C" denote the corresponding I/V waveforms.
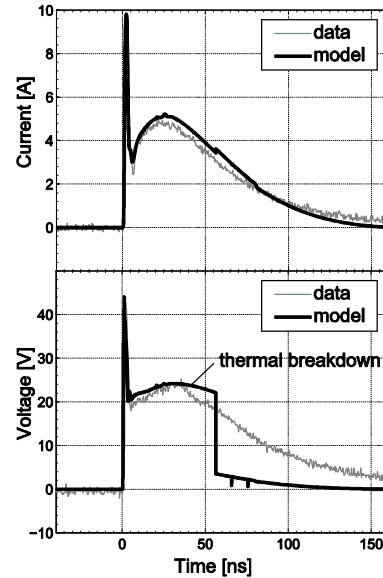

Figure 17: Simulated and measured waveforms for the npn-BJT stressed by GUN-like pulses at 2.5kV GUN level (stress to failure). Thermal failure is observed both in simulation and test.

characteristics (Fig. 15).

For the validation of the device model in reproducing the failure level, the same GUN-like pulse generator as in the study of non-snapping ESD protection elements is applied to the npn-BJT. The device fails thermally at 2.5kV according to both, simulation and measurement (Fig. 17).

As a conclusion for the modeling examples demonstrated in this section, the Wunsch-Bell based

Figure 15: TLP characteristics of the npn-BJT with t_w from 5ns to 0.5µs. R1, R2 represent different R_{on} before and after the triggering of the snapback. Each of R_{on} is a function of t_w.

behavior modeling is widely applicable for different types of ESD devices and circuits. The investigated stand-alone structures are modeled to reproduce self-heating and failure levels which are validated with experimental data.

IV. Application

A. ESD Co-Design on PCB

As the on-chip ESD protection elements are characterized and described in VHDL-AMS, one of the most interesting applications of the models is the prediction of system-level ESD robustness. To achieve the ESD target level of the circuit on board, the co-design of on- and off-chip protection elements is often necessary. Capacitor, varistor, TVS-diode et cetera are commonly employed as off-chip ESD protection elements. Accurate ESD simulations substantially help to select the proper off-chip devices in the system (PCB) design in an early stage of the project.

Combinations of diverse on-chip protection elements with off-chip devices are simulated and measured showing the straightforward application of the proposed modeling methodology. In the simulation setups, a discharge lumped element network including parasitic RLC is used as a common ESD generator (GUN) model.

For the verification by measurements, the on-chip ESD devices introduced earlier are assembled in the plastic package LQFP-64 and placed in a test socket on PCB. The ESD generator TESEQ NSG438 (150pF/330Ω) is used to perform the system-level ESD tests. Fig. 18 shows a fraction of the test board with external devices and the IC socket. Curve trace after each stress is used for monitoring the leakage current as well as for detecting the failure level in the GUN tests.
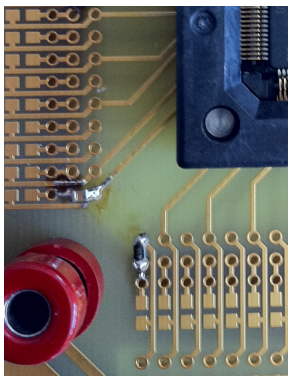

Figure 18: Photograph of the test PCB. Board traces, package and socket parasitics have negligible impact on the system-level ESD robustness in this design.
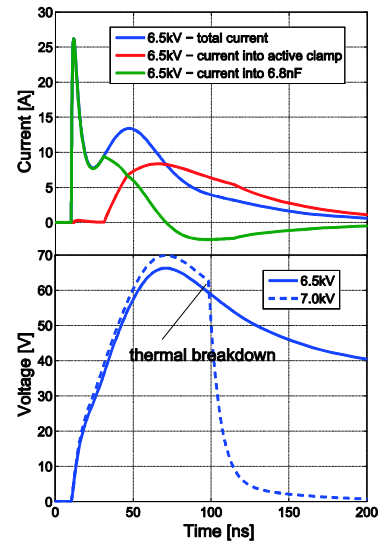

Figure 19: Simulated waveforms of a 6.8nF ceramic capacitor in parallel to an on-chip 25V active clamp under GUN stress. The current distribution is shown at 6.5kV. The failing stress caused by thermal breakdown of the active clamp occurs at 7kV.

The stand-alone active clamp fails electrically at 3kV stress level of GUN-like pulses as discussed in section III. The same failure level is confirmed by real GUN tests using the ESD generator. The simulation predicts an improved total ESD robustness of about 6.5kV in connection with a parallel 6.8nF ceramic capacitor. The on-chip active clamp will fail thermally rather than electrically according to the simulated waveforms (Fig. 19). This result is validated by applying GUN tests where the failure occurs at 6.5kV to 7kV stress levels.

Another example of ESD co-design is implemented by using the 45V pn-diode as on-chip protection. A varistor with typical turn-on voltage of 60V is used as the off-chip ESD device (Fig. 20). The turn-on voltage is a little larger than V_{tr} of the on-chip diode (Fig. 5). Note that the model of the varistor is simply
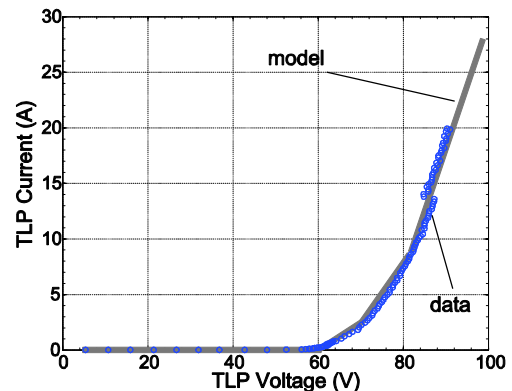

Figure 20: 100ns TLP characteristic of the varistor. The model is generated merely using 100ns TLP without self-heating effect.
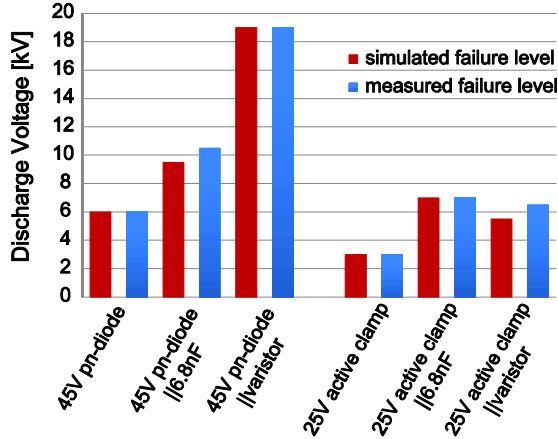
Figure 21: Comparison of simulated and measured failure levels (0.5kV steps) for different combinations with on- and off-chip ESD protections.

Figure 22: Simulated current waveforms of different discharge models showing different pulse duration at 6kV on a 2Ω load.

generated using 100ns TLP curves since the self-heating of off-chip devices is usually not as important as for the on-chip devices due to their very high energy dissipation capability. The stand-alone diode fails at approximately 6kV GUN stress. According to the simulation the failure level of the combined ESD protection will increase significantly to 19kV due to the contribution of the varistor. This is again confirmed by test results.

Fig. 21 summarizes several system-level co-design case studies, clearly showing the possibility to predict the ESD robustness of the protection networks with the Wunsch-Bell based modeling methodology.

B. Various System-Level ESD Discharge Models

Due to the wide range of characterization in pulse width (t_w), the proposed behavior models can also be used to estimate the ESD robustness of the DUTs when applying other system-level pulses such as defined in ISO 10605 [19]. In addition to the discharge model (150pF/330Ω) defined in IEC 61000-4-2, the ISO 10605 standard includes more C/R values such as 330pF/330Ω, 150pF/2kΩ and 330pF/2kΩ, which represent various pulse lengths due to different time constants as depicted in Fig. 22. The shown current waveforms are obtained by simulating a 6kV discharge on a 2Ω load.

The 45V pn-diode and 25V active clamp are used as DUTs in this investigation. Tab. 1 and Tab. 2 show the devices robustness for the different discharge models obtained by simulation and measurement. The measurement results verify the simulation results. Note that for the 45V pn-diode a certain mismatch is observed between data and model for the 330pF/2kΩ
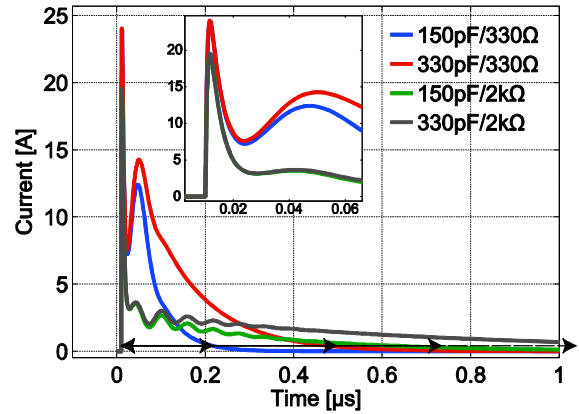
discharge model. The 330pF/2kΩ pulse shows the longest duration, i.e. time constant (Fig. 22). Hence the mismatch gives an indication of the limit of the diode model which is only calibrated up to t_w=1.5µs. This issue however does not affect the results for the active clamp since the device failure is induced by the first peak (electrical fail).

Table 1: Comparison of data and model for the 45V pn-diode stressed by different discharge models according to ISO 10605.

45V pn-diode	Test run	Model		Data	
C/R		Pass	Fail	Pass	Fail
150pF/330Ω	1	5.5kV	5.6kV	5.5kV	6.0kV
330pF/330Ω	1	4.1kV	4.2kV	4.0kV	4.5kV
	2			4.0kV	4.5kV
150pF/2kΩ	1	11.9kV	12.0kV	11.0kV	11.5kV
	2			10.5kV	11.0kV
330pF/2kΩ	1	8.8kV	8.9kV	7.0kV	7.5kV
	2			6.5kV	7.0kV

Table 2: Comparison of data and model for the 25V active clamp stressed by different discharge models according to ISO 10605.

25V active clamp	Test run	Model		Data	
C/R		Pass	Fail	Pass	Fail
150pF/330Ω	1	2.7kV	2.8kV	2.5kV	3.0kV
330pF/330Ω	1	2.7kV	2.8kV	2.5kV	3.0kV
	2			2.5kV	3.0kV
150pF/2kΩ	1	3.4kV	3.5kV	2.5kV	3.0kV
	2			3.0kV	3.5kV
330pF/2kΩ	1	3.4kV	3.5kV	3.0kV	3.5kV
	2			3.0kV	3.5kV

V. Conclusions

The presented behavior modeling method is portable and easy-to-implement. Good correlations between silicon measurements and simulations have been achieved validating the methodology and the models. Details of the application examples including system-level ESD co-design and impact of different pulses on the robustness of the ESD devices are given. During the Wunsch-Bell characterization a wafer-level TLP setup is used which minimizes parasitic effects. In the system-level tests, the parasitic of the used test PCB, package and socket has no significant impact on the robustness of the devices since the models are in most cases valid according to the simulation results. The main advantage of the proposed modeling methodology is the behavior description based on the profound TLP measurements. It avoids the emulation of physical parameters or circuit details which can be arbitrary complicated. The presented methodology easily allows generalizing the modeling method to different types of ESD protection elements. On the other hand, the main drawback of the proposed behavior model is also due to the lack of the physical basis. The self-heating effect is obtained with the fitting function $R_{on}=f(t_w)$ which is derived from the TLP tests. In the reality the pulse waveforms differ usually a lot from the rectangular TLP pulses. Fortunately, most of the real pulses exhibit exponential decay, where at the tale of the pulse the current level is low enough so that the self-heating is not significant anymore. The inaccuracy of the R_{on} estimation in this pulse part is therefore ignorable.

Furthermore, the range of application of the behavior modeling can be extended. In this study, the model is valid up to 1.5μs. An extended characterization up to the milliseconds range enables the simulation of the robustness of protected devices stressed by EOS disturbances such as defined in ISO 7637 [20-22]. Moreover, for on-chip ESD design, with the ESD window given by the circuits being protected, different types of protection schemes can be simulated using the introduced modeling method to achieve the optimal design considering the area consumption and target robustness. The underestimation of the ESD device capability due to models without self-heating (Fig. 1) can lead to ESD overdesign and must be avoided in a cost efficient design.

Acknowledgements

References

[1] W. Li et al., "A Scalable Verilog-A Modeling Method for ESD Protection Devices," in *Proc. EOS/ESD*, 2010, pp. 1A. 1-10.

[2] M. Mayerhofer et al., "ESD Review Methodology using Transient Simulations on Circuit Level and its Application for JEDEC/ESDA HBM and IEC 61000-4-2 Pulses in Automotive Circuits," in *Proc. ESD Forum e.V.,* 2009, pp. 129-139.

[3] D.C. Wunsch and R.R. Bell, "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Voltages," *IEEE Trans. Nuc. Sci.*, NS-15, pp. 244-259, 1968.

[4] V.M. Dwyer, A.J. Franklin and D.S. Campbell, "Thermal Failure in Semiconductor Devices," *Solid-State Electronics,* Vol. 33, No. 5, pp. 553-560, 1990.

[5] B. Deutschmann, et al., "Robustness of ESD Protection Structures against Automotive Transient Disturbances," in *Proc. APEMC*, 2010.

[6] F. Magrini et al., "Correlation between System Level Robustness and TLP Results of ESD Devices," in *IEW*, 2011.

[7] H. Wolf et al., "Pulsed Characterization of a reverse biased pn-Junction for ESD HBM Simulation." *Microelectronics and Reliability*, Vol. 36, Issues 11-12, pp. 1711-1714, 1996.

[8] C. Torres et al., "Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies," in *Proc. EOS/ESD*, 2001.

[9] M. Khazhinsky et al., "ESD Protection for Advanced CMOS SOI Technologies," in *Proc. EOS/ESD*, 2005.

[10] M. Stockinger et al., "Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe," in *Proc. EOS/ESD*, 2006.

[11] L. Lou et al., "An Improved Compact Model of Silicon-Controlled Rectifier (SCR) for Electrostatic Discharge (ESD) Applications," *IEEE Transactions on Electron Devices*, Vol. 55, pp. 3517-3524, 2008.

[12] F. Lafon et al., "ESD Analysis Methodology - From IC Behavior to PCB Prediction," in *Proc. EMC Compo*, 2007, pp. 941-947.

[13] B. Arndt et al., "Simulation based Analysis of ESD Protection Elements on System Level," in *IEW*, 2010.

[14] Y. Cao et al., "A Wunsch-Bell based Behavior Model for On-Chip ESD Devices," in *IEW*, 2011.

[15] IEC International Electro-technical Commission, "Reference number IEC 61000-4-2," Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test, 2001.

[16] Y. Cao et al., "A Failure Levels Study of non-snapback ESD Devices for automotive Applications," in *Proc. IRPS*, 2010, pp. 458-465.

[17] Y. Cao et al., "A TLP-based Human Metal Model ESD-Generator for Device Qualification according to IEC 61000-4-2," in *Proc. APEMC*, 2010.

[18] M. Mergens et al., "ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive," in *Proc. EOS/ESD*, 2006, pp. 54-63.

[19] ISO International Organization for Standardization, "Reference number ISO 10605," Road vehicles - Test methods for electrical disturbances from electrostatic discharge, 2001.

[20] ISO 7637-1:2002(E) "Road vehicles –Electrical disturbances from conduction and coupling – Part 1: Definitions and general considerations," Second edition 2002-03-15, www.iso.ch

[21] ISO 7637-2:2004(E) "Road vehicles –Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only," Second edition 2004-06-15, www.iso.ch

[22] ISO 7637-3:1995(E) "Road vehicles — Electrical disturbance by conduction and coupling — Part 3: Vehicles with nominal 12 V, 24 V or 42 V supply voltage - Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines," 2007