Synthesis of an Optimized Control Signal for an Improved EMC Switching Behavior of MOSFETs Using a System Characterization Approach

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***Abstract*—Active gate control of MOSFETs is a common strategy to improve efficiency and/or electromagnetic compatibility (EMC) of power electronic systems. Finding an appropriate control method for specific requirements is no trivial task, and often there is a trade-off between efficiency and EMC. In this paper, a novel method is proposed that utilizes synthesized control signals. With signal synthesis methods, that can be realized affordable in future integrated circuits, signal shapes can be adjusted more or less arbitrarily. Various requirements, e.g. switching waveforms, overall system's EMC or efficiency, can be aimed at this way. Here, a basic MOSFET circuit is investigated which should generate a specific switching waveform. This waveform shall improve the system's EMC without significantly affecting the efficiency. The system is developed, characterized and a mathematical approximation is derived that respects the important temperature dependency. In this first demonstration, very low switching frequencies are considered that make the reactive elements of the MOSFET negligible. From the requirements and the system model, a suitable control signal can be derived. Measurement and simulation results show the good performance of the proposed method.**

Keywords—power electronics, active emission control, gate control, synthesized control signals

I. INTRODUCTION

Power electronic converters tend to be considerable sources of electromagnetic interferences (EMI). These are mainly caused by the switching transistors. To reduce the high frequency EMI of, e.g., ringing, several methods are known, e.g. an additional gate resistance can be connected between the gate driver and the gate. However, this method usually reduces the slew rate and, therefore, the efficiency of the converter. To resolve this issue, active gate control methods were proposed in [1]-[7]. Different approaches have been developed. In the following, selected methods are discussed.

One possible implementation of active gate control is presented in [1] and [2]. The aim is to improve the EMC-behavior by changing the gate resistance during the switching process. This is realized by a series connection of three programmable gate drivers, whose output resistance is adjustable. Here, three gate drivers are used to control the gate over a wider voltage range. Besides, the gate-source voltage can be shaped more precisely by the use of three drivers, each for a separate voltage range. The gate resistances configuration follows a previously programmed sequence. An alternative, which deals with the influence of the gate resistance, is discussed in [3]. Here, the gate-source voltage is fed back. The gate resistance is controlled by this voltage. The advantage of these methods is the reduction of overshoots and high-frequency signal components in the output spectrum. Whereas, a trade-off between reduction of overshoots, ringing, switching losses and high-frequency disturbances has to be found. If high-frequency disturbances are reduced, the result can be an increase in power dissipation.

In addition, active gate control can be realized by feeding back the gradient of the drain current, as presented in [4]. In this control circuit, the feedback value of the gradient of the drain current is compared with a nominal value, which is estimated on the base of the system parameters. The current gate-source voltage, the load current, technology parameters of the used MOSFET and other parameters are included in the calculation of the nominal value. The gate current is impressed via a controlled current source. A significant reduction of ringing of the drain-source voltage can be achieved, but no reduction of overshoots of u_{DS}.

Different approaches are described in [5] to [7], an additional current is applied to the gate. However, this is realized here by transferring energy from the source path of the MOSFET to the gate path. To do so, the parasitic inductivity of the MOSFET's source path is used and an inductive transducer is built between the source and gate path. By doing so, the gate driver's current is superposed by an additional current supplied by the transducer. As a result, the switching speed and the switching losses are reduced. However, the disadvantages are the increase of overshoots of the drain-source voltage and the usability only for the rising edge.

All of these methods suffer from low flexibility regarding changes in the load circuit. This issue can be resolved by a new method proposed in this paper that applies synthesized control signals to the gate. These signals can be constructed freely in time or frequency domain. By using an appropriate DAC together with sufficient computation power, arbitrary signals can be generated. So, the switching behavior can be controlled very accurately. Since there is no direct feedback of currents or voltages, there is much freedom for the optimization criterion. Possible criterions include efficiency, EMI of an entire power electronic system and specific switching waveforms. Nevertheless, finding the correct control signal is a complex task due to the strongly non-linear system. In this work, two possible approaches are introduced. The first is to determine a mathematical model by characterizing the system. From this model, the necessary control signal is calculated. This approach is pursued in this work. The second option, presented in [8], is an iterative search method. By doing so, the necessary control signal can

be found for any complex system, but the optimization may take some time.

In this work, as shown in Fig. 1, a MOSFET is considered with a given drain-source voltage. To generate this output signal, the necessary gate-source voltage must be determined. This is no trivial task due to the nonlinear behavior of the MOSFET. If a trapezoidal signal with a high slew rate is applied to the gate of the MOSFET, the drain-source voltage can contain ringing as well as over- or undershoots. This can produce disturbing high-frequency signal components, as shown in Fig. 2. An S-shaped curve of the output signal can be desirable. In the studied case, the rise and fall times shall remain unchanged in comparison to the hard switching MOSFET. The concept of using synthesized signals is not new to EMC. In e.g. [9] and [10], synthesized cancellation signals have successfully been applied to suppress the conducted EMI of DC/DC converters.

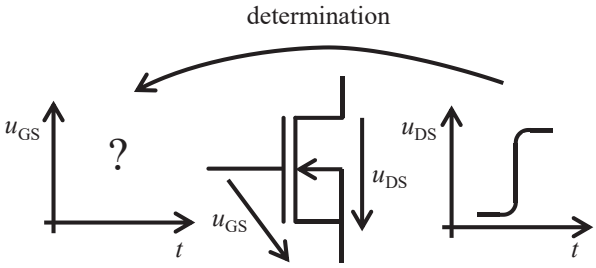

Fig. 1: Concept of the novel strategy of suppression of disturbances

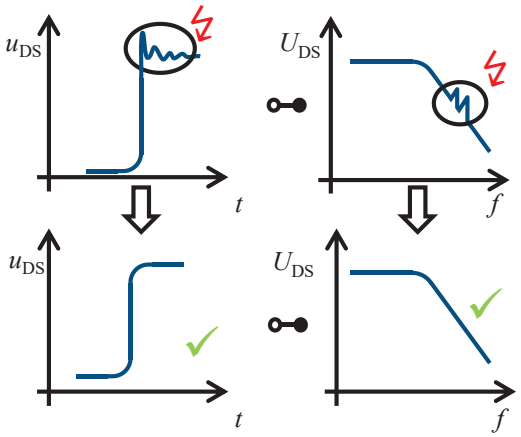

Fig. 2: Suppression of disturbances

At first, the theory of the proposed method is explained in chapter II. In chapter III the method of calculating a control signal to improve the MOSFETs EMC is demonstrated. The generation of a given output signal of a source circuit is explained step by step using a special approximation of the system that respects the temperature dependency of the transistor. The presentation of possible extensions of the discussed method and a summary are finally given.

II. Transistor Control with Synthesized Signals

In this chapter the theory of static transistor control with synthesized signals is explained. Afterwards, this method is transferred to a system whose switching behavior is given. Two possible implementations for finding the appropriate control signals are presented. The first applies a simulation model and the second uses an iterative search approach.

A. Fundamental Theory

The aim of the proposed method is to improve the EMC while keeping the efficiency of a power electronic system. The general approach is depicted in Fig. 3. A synthesizer generates control signals $\overrightarrow{y_e}$ that are passed to the switching devices of the power electronic component. The output quantities $\overrightarrow{y_a}$ can be, e.g., power losses, EMI or switching waveforms. The system function F transfers the inputs $\overrightarrow{y_e}$ to the outputs $\overrightarrow{y_a}$.

$$\overrightarrow{y_a} = F(\overrightarrow{y_e}) \tag{1}$$

By solving (1) for $\overrightarrow{y_e}$, the appropriate control signal is determined.

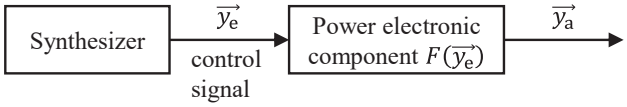

Fig. 3: Principle of shaping the output signal with synthesized control signals

B. Generating a Specific Switching Behavior

To improve both EMC and efficiency, specific signals can be requested as output waveforms. Many power electronic systems operate (quasi-)stationary and cause periodic disturbances. So, there are disturbing harmonics with a spacing of the switching frequency. Therefore, y_a and y_e can be described with a Fourier series. The complex Fourier series of the output signal is given by

$$y_a(t) = \sum_{k=-\infty}^{\infty} c_k \, e^{jk\omega_0 t} \tag{2}$$

with the complex coefficient c_k of the Fourier series, the fundamental angular frequency ω_0 and the time t. The requested output signal can be specified in the frequency domain by the coefficients c_k or in the time domain by a waveform. There are different approaches to determine the necessary control signal. In the following, two of them are discussed.

C. Determination of the Control Signal by Modelling

The first method is to derive a mathematical model of the system using theory, experiment or both. If the found system function is invertible, an analytical solution of the control signal can be found.

From the system function $F(y_e)$ and the requested output signal $y_{a,r}$, the necessary control signal can be determined by (3).

$$y_e = F^{-1}(y_{a,r}). \tag{3}$$

If the inverse function cannot be found or if the determination demands great efforts, a numerical method can be used to calculate the control signal.

D. Determination of the Control Signal by Iteration

The second method works iteratively with the real system. So, there is no need for modelling. This approach is well suited for systems that are too complex to be modeled. The solution can be found by e.g. search or adaptive algorithms.[8]

III. Demonstration

In this chapter, the prior explained method for controlling a transistor via synthesized control signals is applied exemplarily to a real system. At first, the test setup is presented. Further, the used source circuit is characterized to determine the system function. Based on this data, the necessary control signal is calculated. Measurement results show the capability of the presented method.

A. Test Setup

In this work, a simple source circuit is considered. The schematic of the experimental setup can be found in Fig. 4. The input signal y_e corresponds to the internal voltage of the function generator u_C and the output signal y_a represents the drain-source voltage u_{DS}. A n-channel MOSFET BS170 and a load resistance R_2 of 15 Ω are inserted. A constant voltage source is used to provide the supply voltage U_{DC}. The voltage of the control signal is generated via a function generator (Tektronix AFG3101) with the internal resistance $R_i = 50\ \Omega$. The drain-source voltage u_{DS} is measured with an oscilloscope (LeCroy Wavesurfer 3034). The capacitance C represents the parallel connection of blocking capacitors. The resistor R_1 is used as a pull down resistor to ensure the turn-off the MOSFET if there is no signal applied to the gate.

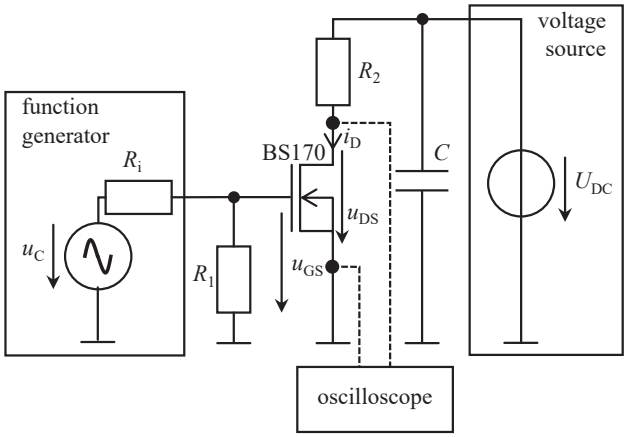

Fig. 4: Schematic of the test setup

If a trapezoidal control signal with a slew rate of 800 ns is set for u_C, the drain-source voltage shown in Fig. 5 is generated. It can be seen that the voltage signal contains small overshoots. To improve the behavior of the MOSFET in this regard, the drain-source voltage should be S-shaped, as shown in Fig. 5. Besides, the slew rate of the drain-source voltage should be kept constant. For this purpose, the corresponding control signal of the MOSFET must be determined.

B. Determination of the System Function

The system function F of the observed system has to be found to calculate the control signal as previously described. To derive the system function, the MOSFET is characterized. Here, the system function describes the relationship between the control signal u_C and the drain-source voltage u_{DS}.

To characterize the MOSFET, the trapezoidal waveform (Fig. 5) is used as test signal for $u_C(t)$ that corresponds to measured drain-source voltage in Fig. 5. This signal reaches over the whole considered voltage range of the control signal (0 V to 5 V). If the measured drain-source voltage u_{DS} is plotted as a function of the related test signal u_C the characteristic curve of the system function in Fig. 6 results.

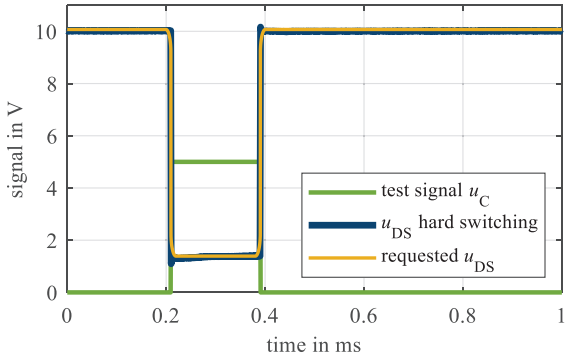

Fig. 5: One period of the test signal, the measured u_{DS} and requested u_{DS}

An approach is to describe the system function by the characteristic equations of the MOSFET and the additional circuitry. In this case, there are basically three equations (cutoff, saturation and ohmic region) that are valid in the respective operation regions. The drain current in the cutoff region is determined by

$$i_D = i_0\, e^{\frac{u_{GS}-U_{th}}{n_0\, U_T}} \tag{4}$$

with the threshold current i_0, the sub-threshold slope factor n_0, the threshold voltage U_{th}, the gate-source voltage u_{GS} and the thermodynamic voltage U_T. In saturation region, the drain current is calculated by

$$i_D = \frac{n}{2}\,(u_{GS} - U_{th})^2 \tag{5}$$

with the slope factor n. The drain current

$$i_D = n\,(u_{GS} - U_{th})\,u_{DS} \tag{6}$$

describes the behavior of the MOSFET in ohmic region. [11]

Thus, the system function cannot be described by one closed analytical equation. Here the EKV-model (**E**nz, **K**rummenacher, **V**ittoz) could be applied to describe the input-output characteristic of the MOSFET. In this model, the behavior of the MOSFET is specified by only one analytical equation that is valid in all regions of operation:

$$i_D = 2\frac{W}{L} n\mu C_{ox} U_T^2 \left[\ln^2\left(1 + e^{\frac{(u_{GS}-U_{th})-nu_S}{2nU_T}}\right) - \ln^2\left(1 + e^{\frac{(u_{GS}-U_{th})-nu_D}{2nU_T}}\right)\right] \tag{7}$$

with the channel width W, the channel length L, the mobility of the current carriers μ, the oxide capacitance C_{ox} and the source-to-bulk voltage u_s as well as the drain-to-bulk voltage u_D [12]. If these equations are used to approximate the drain-source voltage as a function of the gate-source voltage, implicit equations for calculating the drain-source voltage results. As shown in Fig. 6, the match between the approximation of the EKV-model and the measured transfer characteristic is not sufficient.

To simplify the calculation and parameter fitting, the system function can also be approximated by a polynomial. Here powerful tool for finding a best fit are available, e.g. in Matlab. For further investigations a polynomial of 8th order was applied:

$$u_{\mathrm{DS}} = \sum_{k=0}^{8} a_k \, u_{\mathrm{C}}^{k}. \tag{8}$$

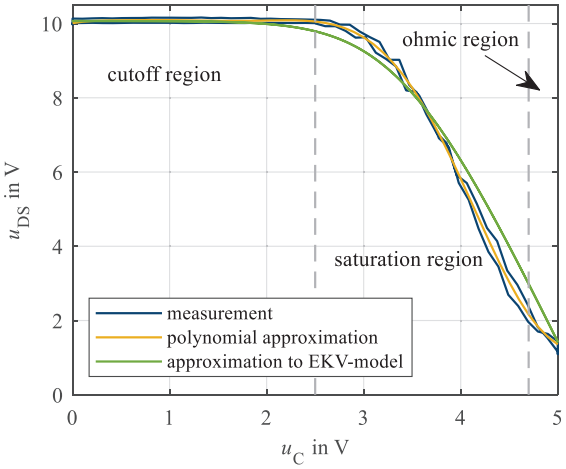

Fig. 6: Measured and approximated system function

Based on this system function the control signal is calculated to generate the S-shaped output signal. Due to the high order of the polynomial, the control signal is found by the iteration rule (9). E.g., a zero search using the Newton-Raphson method with the iteration rule

$$y_{\mathrm{e}}^{\mathrm{n}} = y_{\mathrm{e}}^{\mathrm{n-1}} - \frac{F(y_{\mathrm{e}}^{\mathrm{n-1}}) - y_{\mathrm{a,r}}}{\frac{dF}{dy_{\mathrm{e}}}(y_{\mathrm{e}}^{\mathrm{n-1}})} \tag{9}$$

can be used. For this purpose, the iteration rule from equation (9) can be performed for each point in time until the searched zero point is sufficiently precise. Therefore, the solution is found by the Newton-Raphson method and not analytically. The resulting control signal is depicted in Fig. 7.

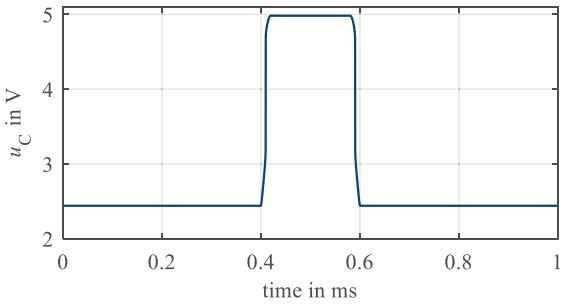

Fig. 7: Calculated control signal

C. *Measurement results*

The control signal determined in the previous section is applied to the gate of the MOSFET using the function generator and the resulting drain-source voltage is measured with an oscilloscope. Considering the measured time domain signal of Fig. 8, it can be seen that overshoots as well as undershoots are significantly reduced. The rise and fall times are kept constant in comparison to the hard switched MOSFET.

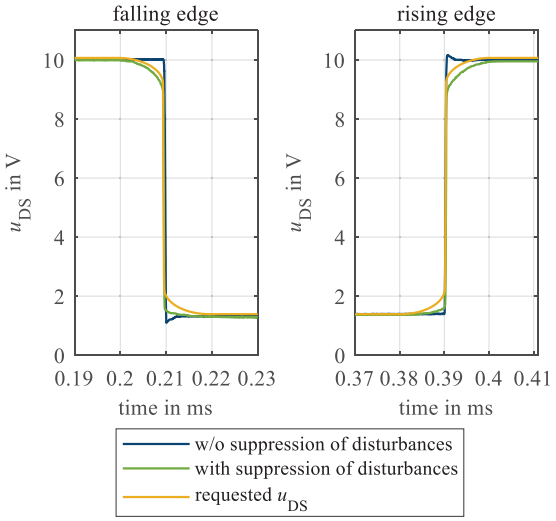

Fig. 8: Measured and requested u_{DS} (time base refers to Fig. 5)

The power losses can be calculated by

$$P_{\mathrm{v}} = \frac{1}{T}\int_{0}^{T} i_{\mathrm{D}}(t) \cdot u_{\mathrm{DS}}(t)\, dt \tag{10}$$

with the period T. The voltage $u_{\mathrm{DS}}(t)$ is measured and the current $i_{\mathrm{D}}(t)$ is calculated by (11).

$$i_{\mathrm{D}}(t) = \frac{U_{\mathrm{DC}} - u_{\mathrm{DS}}(t)}{R_2} \tag{11}$$

Using a trapezoidal test signal the power losses are 106.4 mW. Due to the S-shaped switching waveform the total losses are increased by approximately 0.1 mW . This corresponds to a relative increase of less than 0.1 %.

IV. Thermal Behavior of the Test Setup

If the duty cycle of the requested output signal differs from the one in Fig. 5, the match between the given and measured output signal may become worse (Fig. 12). This is caused by the temperature dependency of the MOSFET. If the power losses are increased, e.g. by an increased duty cycle, the temperature is also increased and the system function of the MOSFET changes. These changes are not negligible. Therefore, the temperature dependency of the MOSFET's system function is analyzed in the following chapter. At first, the system function set is determined. Afterward, the control signal is calculated using the system function corresponding to the expected temperature of the MOSFET. At the end of this chapter, measurements show the need of considering the temperature dependency of the MOSFET.

A. *Determination of the System Function Array*

During operation, the MOSFET and all of the additional circuitry heat up to a thermal equilibrium in dependency of the circuit's power losses. Since the circuitry changes with rising temperature, the system function changes as well. Therefore, the temperature dependency must also be respected in the system function: $u_{\mathrm{DS}}(t) = F(u_{\mathrm{C}}(t), T)$. To characterize the MOSFET, five trapezoidal waveform (Fig. 9) are used as test signals for $u_{\mathrm{C}}(t)$.

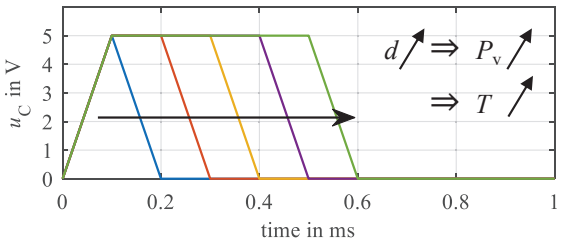

Fig. 9: Test signals to characterize the MOSFET

Here, the total power loss depends not only on the switching losses, but also on the conduction losses. To respect the temperature dependency, different duty cycles are chosen for the five trapezoidal waveforms. An increased duty cycle increases the average conduction losses of the MOSFET and, therefore, the temperature in thermal equilibrium. The MOSFET is tested for five different duty cycles and, therefore, for five different temperatures.

The temperature in thermal equilibrium for the five test signals is measured via a thermographic camera. The average power losses of the MOSFET are calculated by (10) and (11) again. From this data, the correlation between the power losses and the temperature can be found.

Fig. 10 illustrates the corresponding drain-source voltages. The colors of the measured curves refer to the test signals shown in Fig. 9. If the measured drain-source voltages u_{DS} are plotted as a function of the related test signals u_{C} the characteristic curve array of the system function in Fig. 11 results. In this figure can be seen that the drain-source voltage takes different values for the same value of the control signal in dependency of the temperature of the MOSFET. This effect is essentially caused by the thermal behavior of the MOSFET, since the temperature dependency of the threshold voltage and the carrier mobility are dominant [12]. Each characteristic curve of the characteristic curve array is approximated by a polynomial of the order of eight. So, the system function $u_{\mathrm{DS}}(t) = F(u_{\mathrm{C}}(t), T)$ is determined for the complete control voltage range and five different temperatures. To generate the requested output signal as exact as possible, the right system function must be chosen in regard to the expected thermal equilibrium of the MOSFET.

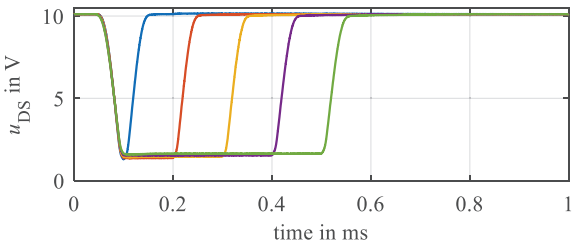

Fig. 10: Measured drain-source voltage u_{DS}

The expected temperature of the MOSFET in thermal equilibrium is determined mathematically based on the demanded $u_{\mathrm{DS}}(t)$. To do so, the expected average power losses are calculated by (10) and (11). The expected temperature is determined by the expected average power losses since the correlation between temperature and power losses is known by characterization.

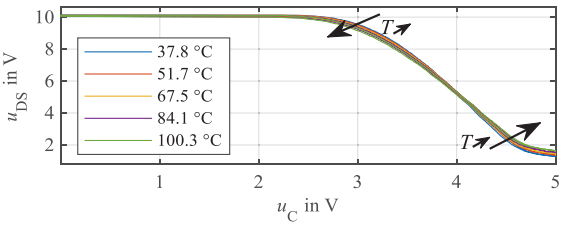

Fig. 11: Transfer characteristic of the MOSFET

B. Determination of Control Signal

In the following, the control signal is determined which achieves the requested output signal depicted in Fig. 12. Basically, four steps are necessary:

1. At first, the expected power losses are calculated by (10) and (11). Here, the power loss is 517.2 mW.
2. The approximation of the temperature as a function of power dissipation is used to calculate the temperature of the MOSFET in thermal equilibrium for the requested drain-source voltage. Here, a temperature of 96.7°C is expected.
3. A fitting system function is chosen. Here, the closest system function is for a temperature of 100.3°C. Therefore, this function is used. If there was no fitting function, interpolation techniques can be applied.
4. At last, the control signal is determined. An analytical solution of (3) is not practicable in this case because the here used polynomials are difficult to invert due to their high order. Therefore, the control signal is calculated numerically using the iteration rule (9).

C. Measurement Results

Fig. 12 shows the requested output signal with a higher duty cycle and voltage range from 4 V to 10 V. Considering the drain-source voltage generated by the control signal estimated with the system function of Fig. 6, the given and measured drain-source voltages do not match well. If the control signal is used from the section before, a better match between the given and measured drain-source voltage is achieved. Here the temperature of the MOSFET in the thermal equilibrium is considered for the given output signal by calculating the control signal. Now, u_{DS} resulted from the correct system function is considered. The difference between the measured u_{DS} and the requested voltage can be explained by the fact that there was no exact match of the expected temperature and the system functions. Furthermore, the calculation of the average power losses is not very precise. Therefore, the temperature of the MOSFET in

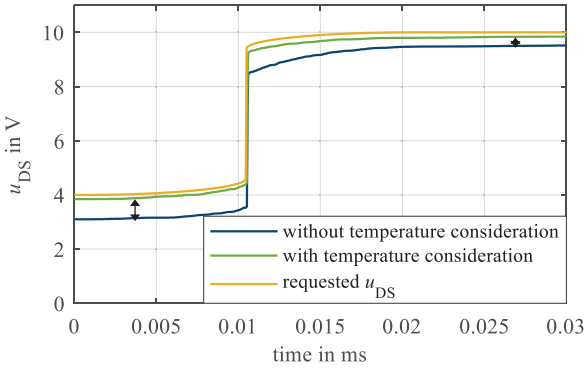

Fig. 12: Measured and requested u_{DS} respecting the temperature of the MOSFET

thermal equilibrium may differ slightly from the mathematical prediction.

V. Simulation Results

In this chapter, based on simulations of the test setup, the capabilities of the method are figured out. The simulation results of the drain-source voltage of a hard switched MOSFET compared to the simulation of the drain-source voltage of a requested S-shaped output signal in frequency domain is shown in Fig. 13. It can be seen that the high frequency signal components of the output signal could be significantly reduced by S-shaped waveforms.

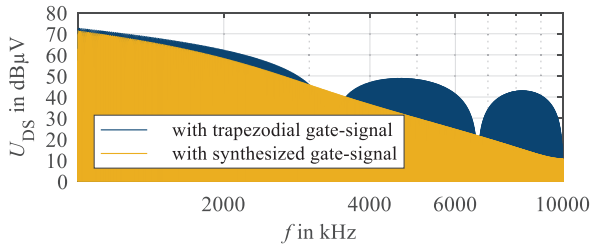

Fig. 13: Simulated u_{DS} with PWM and synthesized gate-signal

In power electronic systems, resonances between passive components (e.g. of the passive EMI filters) can cause narrowband disturbances that are usually hard to mitigate. One possible approach is to reduce the exciting harmonics at the source. This can be done by the presented method. Here, for example, the disturbances in the frequency range of long-wave (150 kHz to 300 kHz) shall be reduced by a synthesized control signal. In Fig. 14 (top), it can be seen that the signal components are significantly suppressed in long-wave range in comparison to the output spectrum of a hard switched MOSFET.

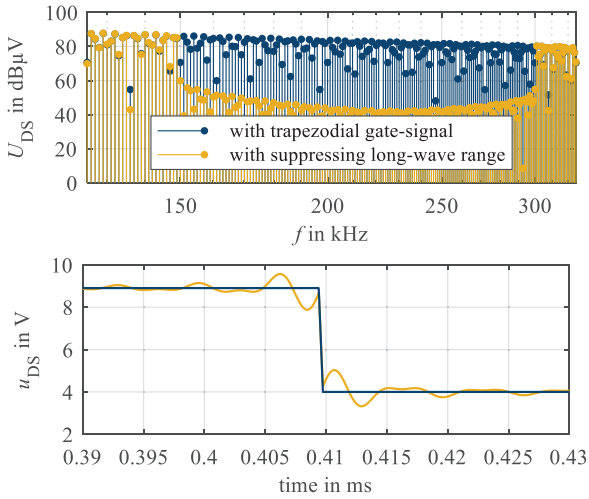

Fig. 14: Simulated u_{DS} with PWM gate-signal and with suppressing the long-wave range in frequency (top) and time domain (bottom)

As shown in Fig. 14 (bottom), suppressing harmonics of the drain-source voltage results in oscillations before and after the switching event. This is similar to the Gibbs phenomenon where cutting off the Fourier series also results in oscillations. Noteworthy, the power losses can increase by a suppression of harmonics. Here, the average power losses before eliminating the long-wave range can be calculated to 824.24 mW by (10) and (11). After suppressing the harmonics in long-wave range, the average power losses are increased by 0.535 mW. So, the additional power losses are negligible in this case.

VI. Conclusion and Outlook

In this work, a new gate control strategy was introduced. Synthesized control signals were applied to a simple MOSFET source circuit to mitigate high frequency contents and keep slew rates of the signals. The desired drain-source voltage shape was specified before. To find the appropriate control signal, a mathematical model was parameterized from measurements. The relevant temperature behavior was considered and the necessary control signal was derived. Measurements and simulation have shown a good match between the requested and the measured drain-source voltage. The proposed method shows great potential to reduce the emissions of power electronic circuits without loss of efficiency. To generate the desired drain-source voltage shape, the temperature of the MOSFET has been considered. The presented approach can be realized with arbitrary waveform generators that can be realized easily today using a microcontroller or FPGA with a digital-to-analog converter.

In this paper, the considered frequency was low and the frequency dependency of the MOSFET could be neglected. In future, MOSFETs at typical switching frequencies shall be considered. In this case, reactive effects (e.g. of capacitances) must be taken into account in the model. Furthermore, the applicability on typical power electronic topologies (e.g. boost converters) shall be investigated.

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